1. A method comprising:

chemical mechanical polishing through a portion of an insulating third layer down to a conductive second layer coated on a first layer having an opening filled at least in part by said third layer.

2. The method of claim 1 including chemical mechanical polishing through the second layer down to the first layer.

3. The method of claim 1 including forming an insulating first layer.

4. The method of claim 3 including covering said first layer with a second layer having a high planarization selectivity relative to the third layer.

5. The method of claim 1 including forming the first layer of oxide and the second layer of tungsten.

6. The method of claim 5 including forming the third layer of high density plasma oxide.

7. The method of claim 1 including conformally coating the walls of said opening with said second layer.

8. The method of claim 1 including forming the third layer of material having lower thermal conductivity than thermally grown oxide.

9. The method of claim 1 including polishing down to said second layer, stopping, and then polishing through a portion of said second layer.

10. A semiconductor structure comprising:

a dielectric material formed over a substrate, said dielectric material having an aperture formed at least partially through said dielectric material;

a conductive material conformally coated over said dielectric and said aperture; and

a thermally insulating material formed within said aperture over said conductive material.

11. The structure of claim 10 wherein said conductive material is tungsten and said insulating material is a high density plasma oxide.

12. The structure of claim 10 wherein said conductive material has high polishing selectivity relative to said insulating material.

13. The structure of claim 10 wherein said insulating material has a lower thermal conductivity than thermally grown oxide.

14. A method comprising:

chemical mechanical polishing through a portion of a thermally insulating third layer down to a conductive layer coated on a first layer having an opening filled at least in part with said third layer;

forming a pair of spaced electrodes so that one of said electrodes is coupled to said conductive layer; and

forming a memory material between said electrodes.

15. The method of claim 14 including forming an electrical contact electrically coupled to a conductive line formed in said substrate.

16. The method of claim 14 including forming the conductive layer by conformally coating said first layer with a conductive material.

17. The method of claim 16 including coating said first layer with tungsten.

18. The method of claim 14 including forming a thermally insulating filler in said opening.

19. The method of claim 14 including planarizing through said thermally insulating third layer using said conductive layer as a planarization stop.

20. The method of claim 19 including stopping the planarizing at said conductive layer and then polishing through said conductive layer to said first layer.

21. The method of claim 14 including planarizing so as to have high selectivity to the conductive layer relative to said third layer.

22. The method of claim 14 including forming a phase change memory material between said electrodes.

23. The method of claim 22 including forming a chalcogenide between said electrodes.

24. A memory comprising:

an electrical contact coupled to a line in a substrate;

a tubular conductor extending upwardly from said contact, said tubular conductor being filled with a thermally insulating material;

a lower electrode coupled to said tubular electrode;

a memory material over said lower electrode; and

an upper electrode over said memory material.

25. The memory of claim 24 wherein said memory material is a phase change material.

26. The memory of claim 25 wherein said phase change material is a chalcogenide.

27. The memory of claim 24 wherein said tubular conductor is formed at least in part of tungsten.

28. The memory of claim 24 wherein said thermally insulating material has a thermal conductivity lower than that of thermally grown oxide.

29. A system comprising:

a processor-based device;

a wireless interface coupled to said processor-based device; and

a semiconductor memory coupled to said device, said memory including a substrate, said substrate including a conductive line, a contact formed over said substrate electrically coupled to said conductive line, and a memory element over said contact, said memory element coupled to said contact by a tubular conductor filled with a thermally insulating material.

30. The system of claim 29 wherein said memory material is a phase change material.

31. The system of claim 30 wherein said phase change material is a chalcogenide.

32. The system of claim 29 wherein said tubular conductor is formed at least in part of tungsten.

33. The system of claim 29 wherein said thermally insulating material has a thermal conductivity lower than that of thermally grown oxide.